BUK9508-55A

TrenchMOS™ logic level FET

22 March 2017 **Product data sheet**

1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology, featuring very low on-state resistance.

2. Features

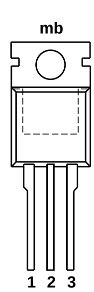
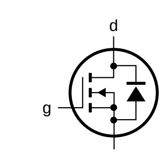
- TrenchMOS™ technology
- Q101 compliant
- 175 °C rated
- Logic level compatible.

3. Applications

- Automotive and general purpose power switching:
  - 12 V and 24 V loads
  - Motors, lamps and solenoids.

4. Pinning information

Table 1: Pinning - SOT78, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	 SOT78A (TO-220AB)	
2	drain (d)		
3	source (s)		
mb	mounting base; connected to drain (d)		

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5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)		-	55	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 5 V	-	125	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	-	253	W
T_j	junction temperature		-	175	°C
R_{DSon}	drain-source on-state resistance	T_j = 25 °C; V_{GS} = 5 V; I_D = 25 A	6.8	8	mΩ
		T_j = 25 °C; V_{GS} = 4.5 V; I_D = 25 A	-	8.5	mΩ
		T_j = 25 °C; V_{GS} = 10 V; I_D = 25 A	6.4	7.5	mΩ

6. Limiting values

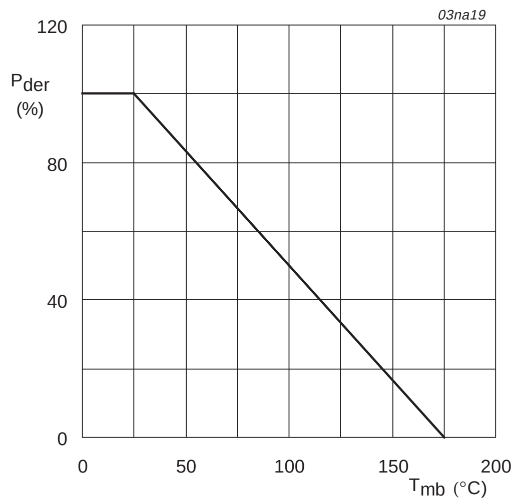
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage (DC)			-	55	V
V_{DGR}	drain-gate voltage (DC)	R_{GS} = 20 kΩ		-	55	V
V_{GS}	gate-source voltage (DC)			-	±15	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 5 V; Figure 2 and 3	[1]	-	125	A
			[2]	-	75	A
		T_{mb} = 100 °C; V_{GS} = 5 V; Figure 2	[2]	-	75	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs; Figure 3		-	503	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1		-	253	W
T_{stg}	storage temperature			–55	+175	°C
T_j	junction temperature			–55	+175	°C
Source-drain diode						
I_{DR}	reverse drain current (DC)	T_{mb} = 25 °C	[1]	-	125	A
			[2]	-	75	A
I_{DRM}	peak reverse drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs		-	503	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 75 A; $V_{DS} \leq 55$ V; V_{GS} = 5 V; R_{GS} = 50 Ω; starting T_{mb} = 25 °C		-	670	mJ

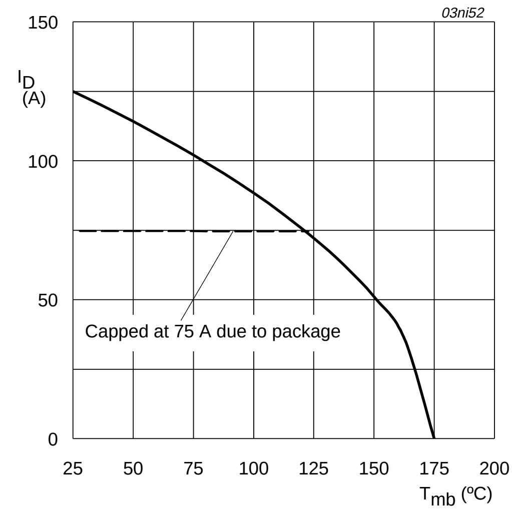
[1] Current is limited by power dissipation chip rating

[2] Continuous current is limited by package.



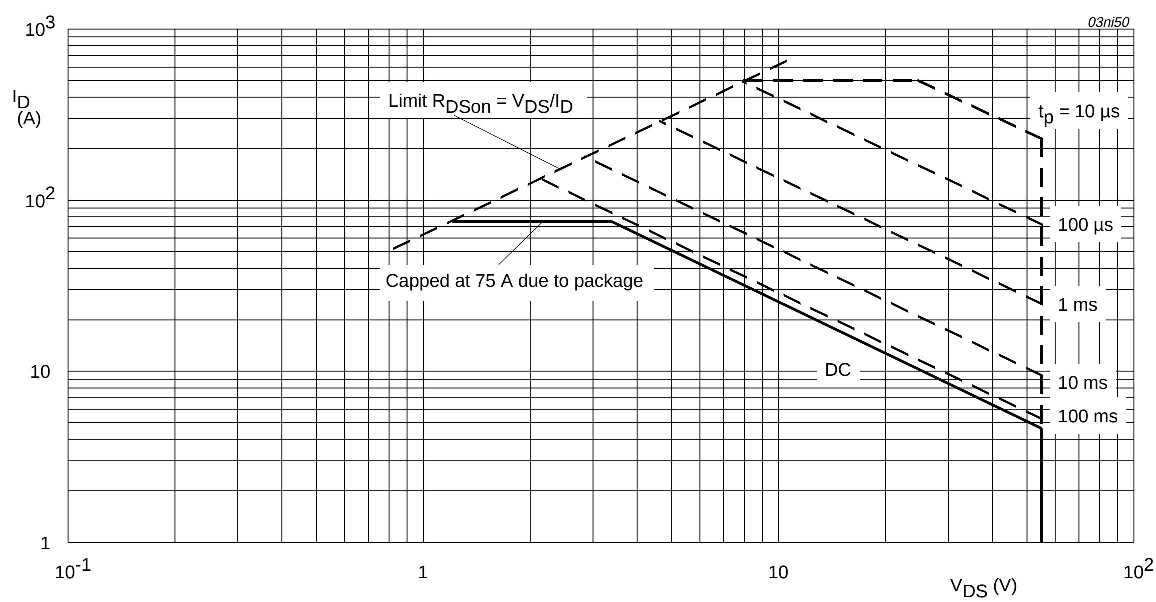
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 4.5$ V

Fig 2. Continuous drain current as a function of mounting base temperature.



$T_{mb} = 25$ °C; I_{DM} single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.59	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78	vertical in still air	-	60	-	K/W
	SOT404	mounted on a printed circuit board; minimum footprint	-	50	-	K/W

7.1 Transient thermal impedance

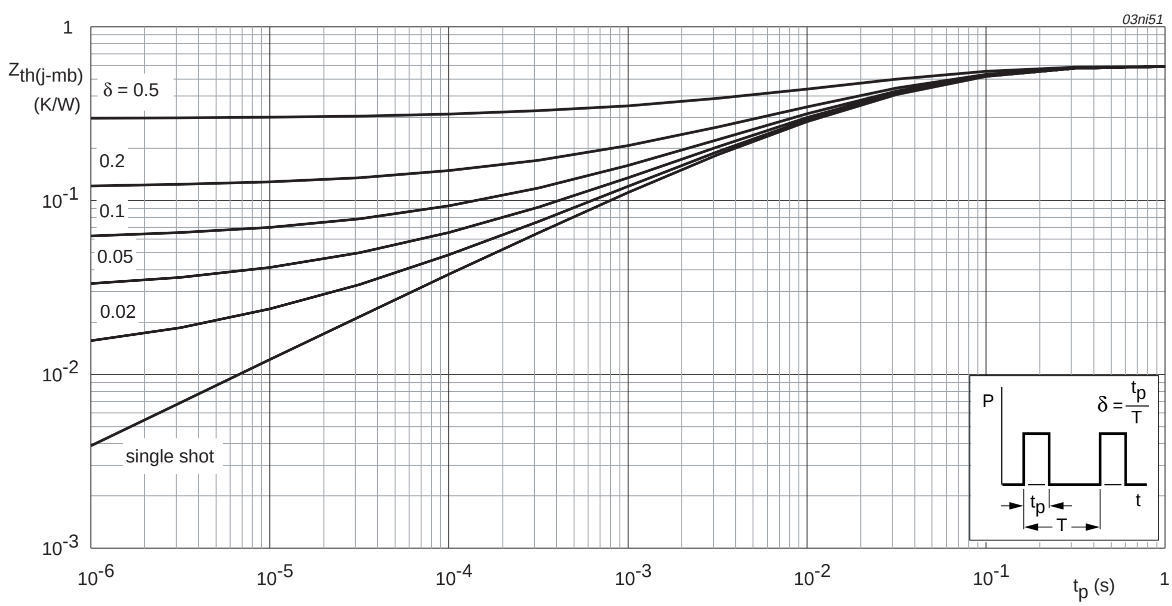


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

Table 5: Characteristics

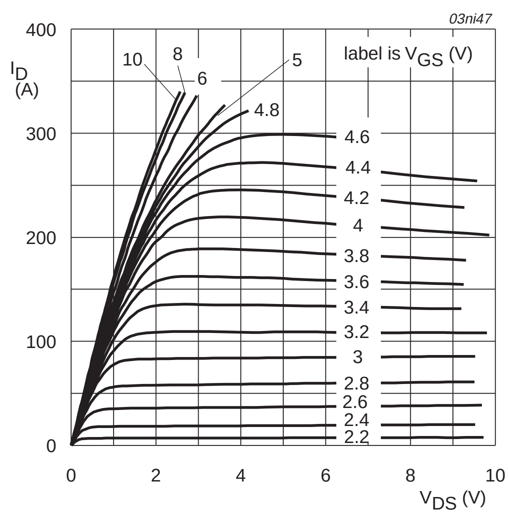
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V				
		T_j = 25 °C	55	-	-	V
		T_j = –55 °C	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9				
		T_j = 25 °C	1	1.5	2	V
		T_j = 175 °C	0.5	-	-	V
		T_j = –55 °C	-	-	2.3	V
I_{DSS}	drain-source leakage current	V_{DS} = 55 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.05	10	µA
		T_j = 175 °C	-	-	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A; Figure 7 and 8				
		T_j = 25 °C	-	6.8	8	mΩ
		T_j = 175 °C	-	-	16	mΩ
		V_{GS} = 4.5 V; I_D = 25 A	-	-	8.5	mΩ
		V_{GS} = 10 V; I_D = 25 A	-	6.4	7.5	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	V_{GS} = 5 V; V_{DD} = 44 V; I_D = 25 A; Figure 14	-	92	-	nC
Q_{gs}	gate-to-source charge		-	11	-	nC
Q_{gd}	gate-to-drain (Miller) charge		-	43	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 12	-	4551	6021	pF
C_{oss}	output capacitance		-	760	900	pF
C_{rss}	reverse transfer capacitance		-	500	687	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; R_G = 10 Ω	-	40	-	ns
t_r	rise time		-	175	-	ns
$t_{d(off)}$	turn-off delay time		-	280	-	ns
t_f	fall time		-	167	-	ns
L_d	internal drain inductance	from drain lead 6 mm from package to centre of die	-	4.5	-	nH
		from contact screw on mounting base to centre of die SOT78	-	3.5	-	nH
		from upper edge of drain mounting base to centre of die SOT404	-	2.5	-	nH
L_s	internal source inductance	from source lead to source bond pad	-	7.5	-	nH

Table 5: Characteristics...*continued*

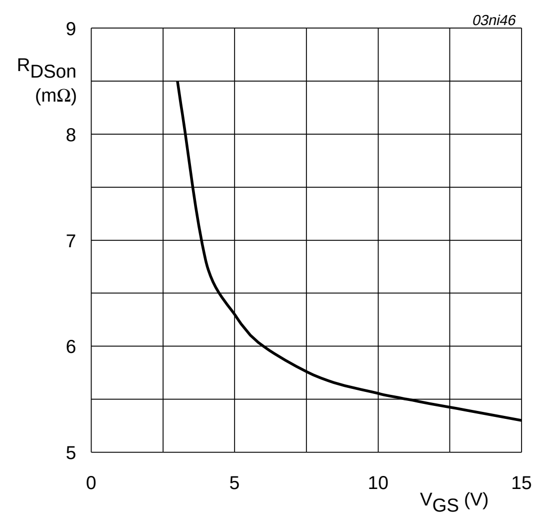
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 25 A; V_{GS} = 0 V; Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 75 A; dI_S/dt = –100 A/µs V_{GS} = –10 V; V_{DS} = 25 V	-	70	-	ns
Q_r	recovered charge		-	170	-	nC



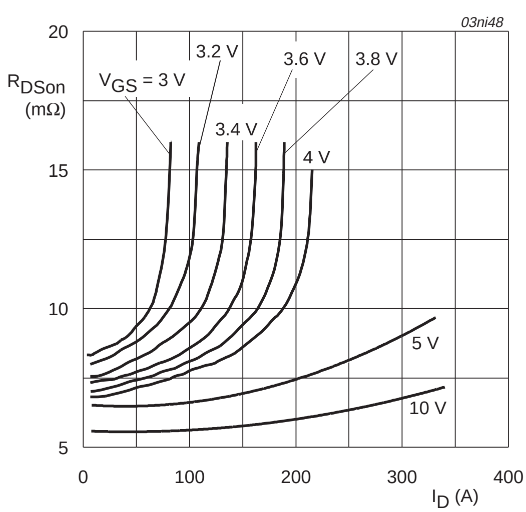
T_j = 25 °C; t_p = 300 µs

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



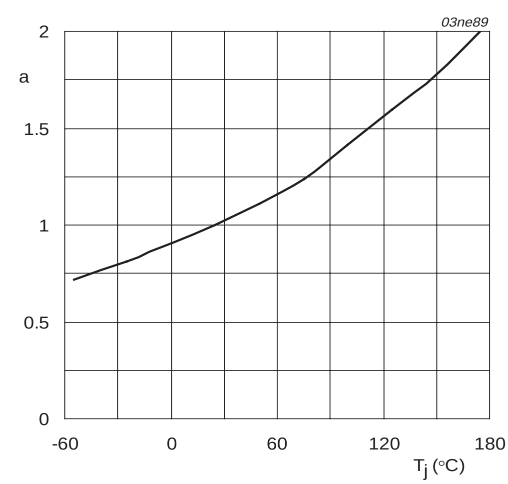
T_j = 25 °C; I_D = 25 A

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



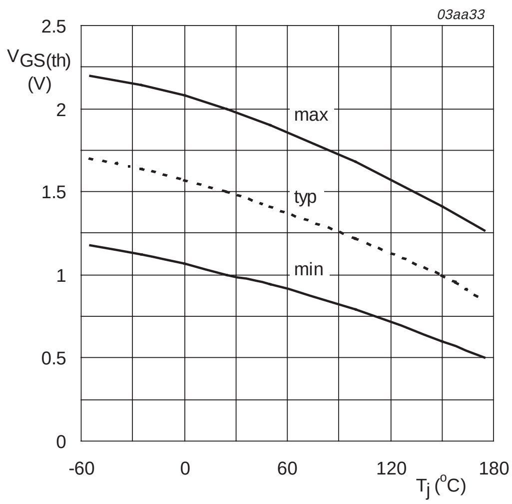
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



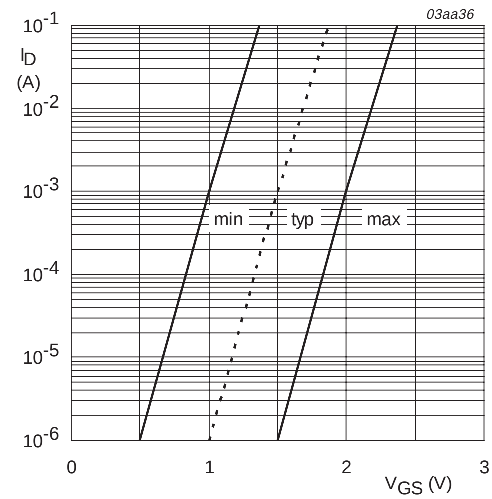
a = $R_{DSon}/R_{DSon(25\,°C)}$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



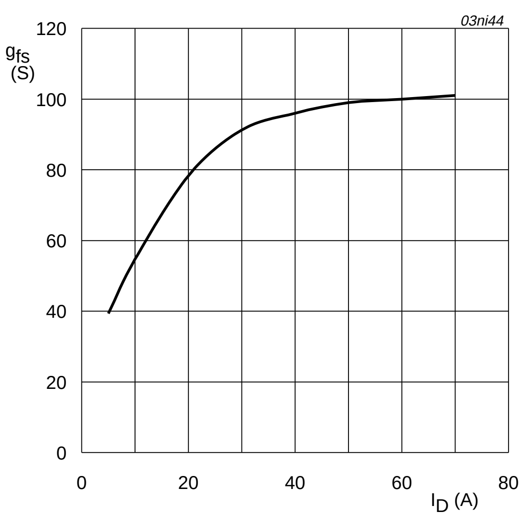
I_D = 1 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature.



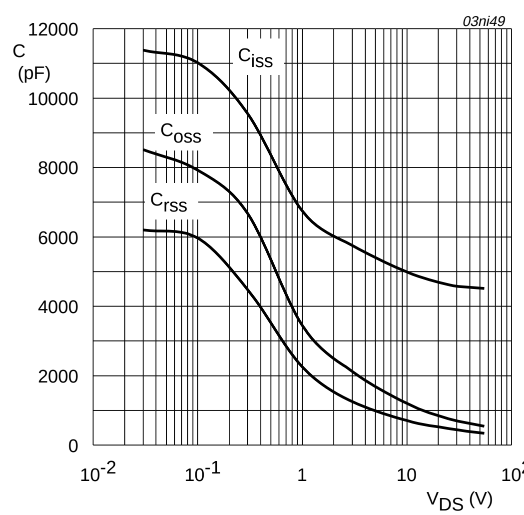
T_j = 25 °C; V_{DS} = V_{GS}

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



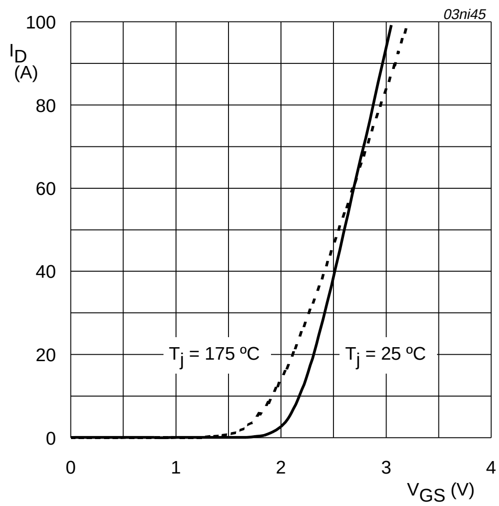
T_j = 25 °C; V_{DS} = 25 V

Fig 11. Forward transconductance as a function of drain current; typical values.



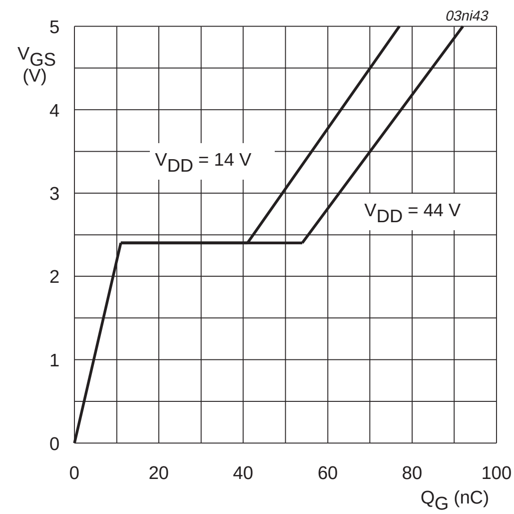
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



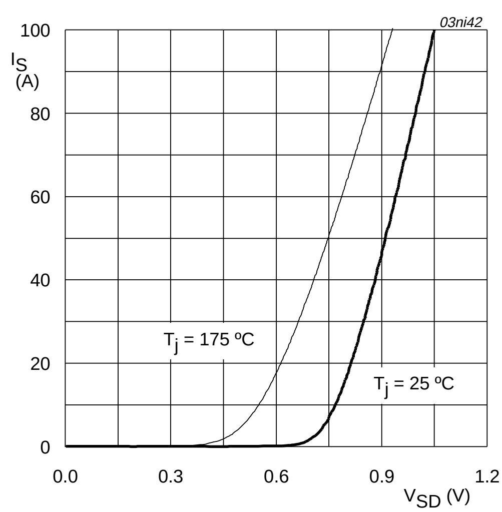
V_{DS} = 25 V

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



T_j = 25 °C; I_D = 25 A

Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.

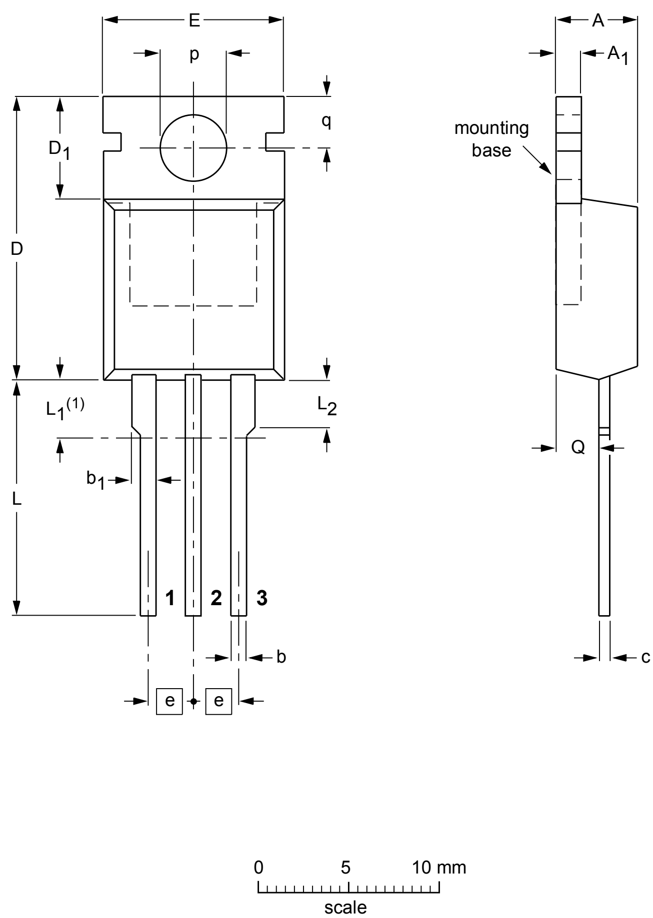


V_{GS} = 0 V

Fig 15. Reverse diode current as a function of reverse diode voltage; typical values.

9. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78A**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	$L_1^{(1)}$	L_2 max.	p	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.6	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78A		3-lead TO-220AB	SC-46			~~03-01-22~~ 05-03-14

Fig. 16. Package outline TO-220AB (SOT78A)

10. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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